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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

#17 Appeal Brief
M. Baumson
1/6/04

IN RE APPLICATION OF	:	
TOSHIAKI SHINOHARA	:	EXAMINER: NGUYEN, D. P.
SERIAL NO: 09/895,319	:	
FILED: JULY 2, 2001	:	GROUP ART UNIT: 2814
FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME	:	

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicants hereby appeal the outstanding Final Rejection of March 24, 2003.

REAL PARTY IN INTEREST

The real party in interest in the above-identified application is Mitsubishi Denki Kabushiki Kaisha having a place of business at 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100-8310 Japan.

RELATED APPEALS AND INTERFERENCES

Applicant and Applicant's representative are not aware of any related appeals or interferences that would directly effect or be directly affected by or have a bearing on the board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-8 are the pending claims and Claims 1-7 are being appealed. Claim 8 was indicated as allowable if rewritten in independent form.

Claims 9-11 were canceled during prosecution of the above-identified application.

STATUS OF AMENDMENTS

No amendments were filed subsequent to the Final Rejection of March 24, 2003.

A Response requesting reconsideration of the outstanding Final Rejection was filed on June 23, 2003. The Advisory Action of July 8, 2003, indicated that Response requesting reconsideration did not place the application in condition for allowance.

SUMMARY OF THE INVENTION

The claimed invention is directed to a semiconductor device having a metal block for dissipating heat. Non-limiting examples of the present invention are shown in Figures 1 and

2B of the present specification (see also the discussion in the present specification at page 10, line 1 *et seq*).

The semiconductor device includes, and with reference to Figure 1 as a non-limiting example, a semiconductor element (1), a lead frame (2a) having a first surface on which the semiconductor element (1) is mounted and a second surface opposite to the first surface, and a metal block (5). The metal block (5) is formed on the second surface of the lead frame (2a), and an insulation layer (7) is formed on the metal block (5), opposite to the lead frame (2a). Further, a bonding material (10) is formed between the second surface of the lead frame (2a) and the metal block (5) and the bonding material (10) has a higher heat conduction than the insulation layer (7).

As a further feature, the metal block (5) is disposed in opposed relation to the semiconductor element (1) and the metal block (5) has a wider surface opposite the bonding material (10) than the bonding material (10) (see, for example, the present specification at page 10, line 17, to page 11, line 3).

As a further feature, the semiconductor element includes a plurality of semiconductor elements and the metal block (5) is separate for each insulated unit between the semiconductor elements. Further, a resin package (6) is configured to seal the semiconductor element (1), the lead frame (2a), and the metal block (5) while uncovering the insulation layer (7), and the insulation layer (7) has a higher heat conduction than the resin package (6).

As a further feature, the semiconductor device has an insulation layer (7) that includes a base material with a same base as the resin package (6), and a ceramic powder. Further, the metal block (5) has a first surface and a second surface opposite to the insulation layer (7), the first surface of the metal block (5) is closer, as viewed in a vertical direction, to the lead frame (2a) than is the second surface of the metal block (5), and the bonding material (10)

lies between the second surface of the lead frame (2a) and the first surface of the metal block (5) (see, for example, the present specification at page 11, line 9, to page 12, line 9).

As a further feature, the lead frame (2a) has a third surface on a same side as the second surface, the third surface is closer, as viewed in a vertical direction, to the semiconductor element (1) than is the second surface, and an insulation space (60) is defined between the metal block (5) and the third surface.

ISSUES

The only issue pending in the outstanding Final Rejection is whether the combination of teachings in U.S. Patent No. 5,767,573 to Noda et al. (herein "Noda") in view of the teachings in U.S. Patent No. 6,297,959 B1 to Ueno et al. (herein "Ueno") renders obvious the subject matter of Claims 1-7.

GROUPING OF CLAIMS

Claims 1-7 are grouped together and thereby stand and fall together. Claim 8 is allowable if rewritten in independent form.

ARGUMENT

Independent Claim 1 positively recites "a metal block on said second surface of said lead frame." Such a feature positively recited in the independent claim, and thereby the claims depending therefrom, clearly distinguishes over the applied art of Noda in view of Ueno for the reasons further discussed below.

The Final Rejection of March 24, 2003, relies on the teachings of Noda to disclose each of the claimed features except a metal block. The Final Rejection states at page 2, line

22, "Noda et al. fail to disclose the circuit pattern layer 106 is a metal block." To overcome that recognized deficiency in Noda, the Final Rejection cites the teachings in Ueno in Figure 2 to teach a radiator 41 that provides a radiation structure for a heating element which can prevent the leakage of silicon grease.[1]

However, the above-noted rejection is improper as the noted teachings in Ueno are not properly applicable to the teachings in Noda because the teachings in Ueno are not directed to the same type of layer as in Noda.

In more detail, Noda discloses in Figure 1 a semiconductor element 101 formed on a lead frame 103a that is formed on a pattern layer 106. Further, the pattern layer 106 is formed on an insulating layer 105 and the insulator layer 105 is formed on a heat sink 104. The Final Office Action of March 24, 2003, identifies the pattern layer 106 shown in Figure 1 in Noda with a metal block claimed in independent Claim 1. However, Noda discloses at column 9, line 63, to column 10, line 6, that the heat sink 104 improves heat dissipation characteristics of a whole semiconductor device. Further, Noda clearly shows in Figure 1 the pattern layer 106 as a thin layer and discloses at column 10, lines 2-3, that "the circuit pattern layer 106 is formed of ... cladding foils." Accordingly, the pattern layer 106 does not inherently have a function of dissipating heat, i.e., layer 106 does not have a function of spreading heat in a vertical direction with respect to a thickness of the circuit pattern layer 106. Furthermore, the circuit pattern layer 106 in Noda functions as an electric circuit pattern designed to ***transmit electrical signals*** and does not provide good heat dissipation. Rather, the heat sink 104 of Noda provides the heat dissipation function for the semiconductor device.

[1] Final Rejection of March 24, 2003, paragraph bridging pages 2 and 3.

Ueno shows in Figure 1 a radiator 41 that dissipates heat from a power element 1. Therefore, the heat sink 104 in Noda and the radiator 41 of Ueno have a similar function of dissipating heat from the power element. However, the circuit pattern layer 106 of Noda and the radiator 41 of Ueno do ***not*** have ***similar functions***, in contrast to the statements in the Final Rejection of March 24, 2003. Therefore, it is respectfully submitted that one of ordinary skill in the art would not have replaced the circuit pattern layer 106 in Noda with the radiator 41 in Ueno because these two elements are used for different scopes.

Moreover, MPEP § 2143.01 states that a statement that a modification of the prior art to meet the claimed invention would have been well within the ordinary skill of the art at the time the claim invention was made . . . is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings (modify the teachings) of the references. Since the suggestion or motivation to one skilled in the art to replace the thin element provided to transmit the electrical signal in Noda with the thick element provided to diffuse heat in Ueno is not objectively admitted in Noda or Ueno, a *prima facie* case of obviousness cannot be established in view of MPEP § 2143.01.

In such ways, it is respectfully submitted that the combination of Noda and Ueno fails to teach or suggest the claimed metal block, and that no *prima facie* case of obviousness has been established in that respect.

Moreover, it is only the Applicants of the present invention who have recognized any benefits of the metal block (5) formed between the lead frame (2a) and the insulation layer (7), such that heat generated from the power element (1) is diffused in the vertical direction with respect to the thickness of the metal block (5) by the metal block (5), and such that an

area over which heat passes through the insulation layer (7) is greater than in the devices of the background art.[2]

In maintaining the outstanding rejection, the Advisory Action of July 8, 2003, states "the circuit pattern 106 has the function of dissipating heat." That statement is incorrect, as discussed above. Further, the Advisory Action states that features upon which the Applicants rely "the heat generated from the power element is diffused in the vertical direction with respect to the thickness of the metal block by the metal block" are not recited by the claims. Applicants respectfully submit that the metal block (5) inherently has the advantage of diffusing heat in a vertical direction, and that inherent advantage is not and cannot be achieved by the proposed combination of teachings in Noda and Ueno.

In view of the foregoing comments, it is respectfully submitted that the pending claims on appeal patentably distinguish over the combination of teachings of Noda and Ueno.

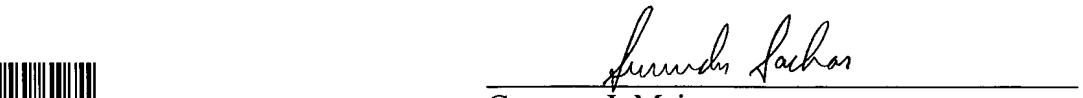
[2] See specification, page 12, line 21, to page 13, line 5.

CONCLUSION

It is respectfully submitted that the outstanding rejection is improper, and that therefore the outstanding rejection must be REVERSED.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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APPENDIX

Claim 1 (Previously Presented): A semiconductor device comprising:

a semiconductor element;

a lead frame having a first surface on which said semiconductor element is mounted, and a second surface opposite to said first surface;

a metal block on said second surface of said lead frame;

an insulation layer on said metal block opposite said lead frame; and

a bonding material between said second surface of said lead frame and said metal block,

wherein said bonding material has a higher heat conduction than said insulation layer.

Claim 2 (Original): The semiconductor device according to claim 1,

wherein said metal block is disposed in opposed relation to said semiconductor element.

Claim 3 (Previously Presented): The semiconductor device according to claim 1,

wherein said metal block has a wider surface opposite said bonding material than said bonding material.

Claim 4 (Original): The semiconductor device according to claim 1,

wherein said semiconductor element includes a plurality of semiconductor elements, and

wherein said metal block is separate for each insulated unit between said semiconductor elements, and is provided in corresponding relation to at least one of said semiconductor elements.

Claim 5 (Previously Presented): The semiconductor device according to claim 1, further comprising:

a resin package configured to seal said semiconductor element, said lead frame and said metal block while uncovering said insulation layer,

wherein said insulation layer has a higher heat conduction than said resin package.

Claim 6 (Previously Presented): The semiconductor device according to claim 5,

wherein said insulation layer comprises a base material with a same base as said resin package, and ceramic powder.

Claim 7 (Previously Presented): The semiconductor device according to claim 1,

wherein said metal block has a first surface and a second surface opposite said insulation layer,

wherein said first surface of said metal block is closer, as viewed in a vertical direction, to said lead frame than is said second surface of said metal block, and

wherein said bonding material lies between said second surface of said lead frame and said first surface of said metal block.

Claim 8 (Previously Presented): The semiconductor device according to claim 1,

wherein said lead frame has a third surface on the same side as said second surface,

wherein said third surface is closer, as viewed in a vertical direction, to said semiconductor element than is said second surface, and

wherein an insulation space is defined between said metal block and said third surface.

Claims 9-11 (Canceled)